

Appl.No. 09/816,923

Amdt. dated June 10, 2004

Reply to Office action of May 12, 2004

Remarks

Reconsideration of the application is requested.

Claims 1-11 remain in the application. None of the claims have been amended.

We begin with the rejection of claims 1-3 and 7-9 as allegedly being anticipated by *Ting et al.* (US 5,969,422, hereinafter "Ting") under 35 U.S.C. § 102. The rejection is in error and we respectfully traverse.

While it is appreciated that the Examiner has modified his interpretation of the reference *Ting*, the rejection is still clearly unwarranted. In addition, it is questionable whether the finality of the latest action - given that the rejection has been modified - is not premature. The Examiner had originally read the claimed "spacers" on the structure 14 of *Ting*. According to the modified rejection, the structure 22 is now used as the allegedly anticipatory element in the reference.

Upon reviewing the disclosure of *Ting*, the new interpretation is even more far-fetched than the old reading. The seed layer wall 22 of *Ting* cannot possibly read on the claimed "spacers

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acting as a barrier to diffusion of a material from said first conductive structure into said second insulating layer."

In an interpretation most favorable to the Examiner's position, the structure of Ting's Fig. 2 would receive these labels, drawn from applicant's claims:

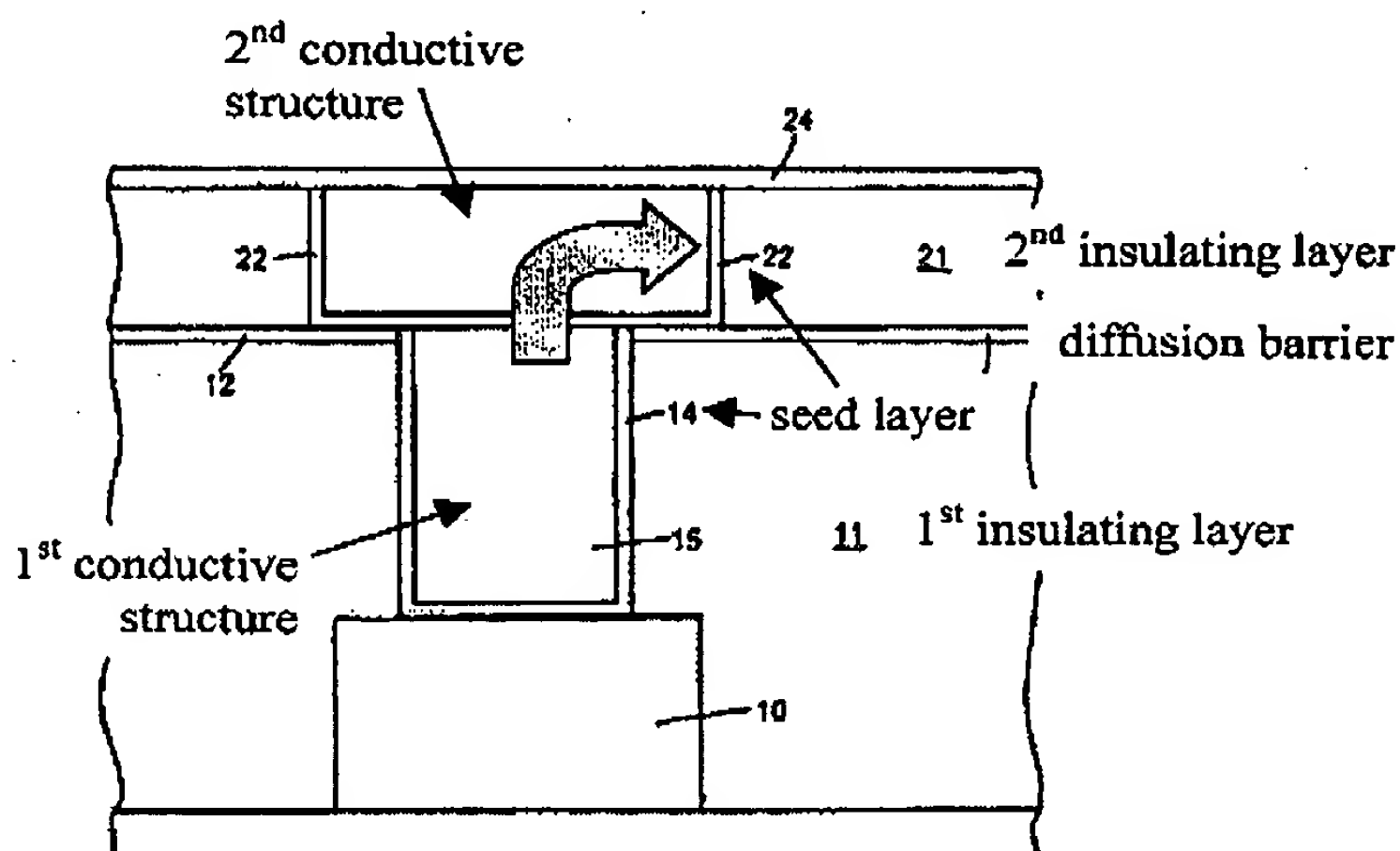


FIG. 2

The seed layer 22 is described as a "catalytically active CU-refractory metal alloy seed layer." Col. 9, lines 22-23.

Further, Ting states that "[t]he seed layer alloy advantageously serves not only as a catalyst or base metal for subsequent electroless plating or electroplating, but as a diffusion barrier preventing Cu from diffusing through the underlying dielectric material." It follows that the layer 22 may indeed be referred to as a diffusion barrier. HOWEVER, if

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the layer 22 is a barrier, the material from the first conductive structure 15 CANNOT POSSIBLY reach the vertical parts of the layer 22 at the side walls of the contact hole above. First, the material would be stopped by the horizontal layer 22, and second it would have to diffuse through the entire second conductive structure 23. This impossible diffusion is illustrated with the shaded arrow in Fig. 2 above.

Ting cannot anticipate the invention defined in claims 1-3 and 7-9. Anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well as disclosing structure which is capable of performing the recited functional limitations. RCA Corp. v. Applied Digital Data Sys., Inc., 730 F.2d 1440, 221 USPQ 385 (Fed. Cir. 1984); W.L. Gore and Assoc., Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983).

Ting does not show the required "spacers" on the side walls of the upper contact hole that would be capable of performing the recited function (i.e., to prevent material from the first conductive structure to diffuse into the upper dielectric).

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Having thus overcome the anticipation rejection, we will now address the obviousness rejection. Claims 4-6, 10, and 11 have been rejected as being obvious over Ting under 35 U.S.C. § 103. We respectfully traverse.

The Examiner stated that these claims are rejected "as far as understood." This statement is unacceptable. If the claims are not properly understood or understandable, the Examiner should reject the claims under 35 U.S.C. § 112 or at least object to the claims and request that applicant explain. The Examiner is requested to rescind the insert "as far as understood."

Further, the Examiner's summary of the allegedly critical issue appearing on page 3 is entirely misplaced. The invention and the application have absolutely nothing to do with the issues dealt with in either Howard v. Detroit Stove Works, 150 U.S. 164 (1893), or In re Larson, 144 USPQ 347 (CCPA 1965), or In re Fridolph, 135 USPQ 319 (CCPA 1962). The issue of multiplication of elements or integration of multiple elements into one is a concept that has no bearing on superfine

structures in integrated circuits. We are dealing here with semiconductor processing and microscopic integration. Also, we are dealing here with objects that have to do with developing

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procedures and structures that allow new materials to be utilized in the integration of semiconductor circuits. The Examiner is respectfully urged to reconsider the applicability of these cases.

More importantly, even, the Examiner is earnestly urged to reconsider the conclusory statement that the use of spacers and the second diffusion barrier layer is simply a matter of engineering choice, as a corollary to the cited cases. Nothing could be more far-fetched, and indeed more denigrating to the art of semiconductor manufacture, than the application of these macro-mechanical multiplication concepts to the case at hand.

Neither Ting nor any other reference of record, whether taken alone or in combination, shows or suggests the features defined in claims 1 and 7, or in the dependent claims. All of the claims are patentable over the art.

In view of the foregoing, reconsideration and allowance of claims 1-11 are solicited.

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If an extension of time is required, petition for extension is herewith made. Please charge any fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,



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